	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	132	harari near eliyahou.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 15:55	
2	BRS	L2	125	1 and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 15:55	
3	BRS	L3	88	2 and substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:11	
4	BRS	L4	34	yuan near jack.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:11	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	34	4 and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:11	
6	BRS	L6	30	5 and substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:14	
7	BRS	L7	23	fong near yupin.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:16	
8	BRS	L8	14	samachisa near george.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:17	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	4	6103573.pn. or 6151248.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:19	
10	BRS	L10	1	"09667344"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:19	
11	BRS	L11	1262	438/257.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:19	
12	BRS	L12	357	11 and (dielectric near10 substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/14 16:20	

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	☐	☐	US 6151248 A	Dual floating gate EEPROM cell array with steering gates shared by adjacent cells	365/185.14	18	20001121
2	☐	☐	US 6103573 A	Processing techniques for making a dual floating gate EEPROM cell array	438/257	21	20000815
3	☒	☐	US 6151248 A	Flash EEPROM cell array has elongate source-drain diffusions and steering gates arranged in spaces between alternate floating gate rows, such that it extends across substrate in Y-direction		18	20001121
4	☒	☐	US 6103573 A	Making a non-volatile memory on a semiconductor substrate involves forming steering gates with widths that extend over and being capacitively coupled with two adjacent floating gates		21	20000815